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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,704	12/09/2003	Stefan Marinca	H0682.70000 US00	5247

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EXAMINER	
LAXTON, GARY L	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 05/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,704	MARINCA, STEFAN	
	Examiner	Art Unit	
	Gary L. Laxton	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19* is/are allowed.

6)☒ Claim(s) *1 and 20* is/are rejected.

7)☒ Claim(s) *2-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/11/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1 and 20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Mizuide (US 5,789,906).

Mizuide discloses a conventional reference voltage generating circuit in FIG. 1. The conventional circuit consists of a widlar current mirror circuit 500 including two transistors Q1 and Q2 and a resistor R2; two resistors R1 and R3 connected to two nodes N1 and N3, respectively; a current source I for supplying a current to these resistors R1 and R3, respectively; and an operational amplifier (OP amp) having two input terminals connected to the two nodes N1 and N3, respectively and an output terminal VBG for outputting a reference voltage. Further, the output terminal VBG is fed back to a node N2. The emitter area of the transistor Q2 is designed to be an integer times larger than that of the transistor Q1.

The current supplied by the constant current source I is divided into I1 and I3. Further, the remaining current thereof is absorbed by the OP amp 600. When the OP amp 600 is activated, the current I3 is supplied to the widlar current mirror circuit 500, and the current I1 controlled by the widlar current mirror circuit 500 flows through the resistor R1. Therefore, a potential difference R1.times.I1 can be generated across the resistor R1. Further, a potential V3 at the node N3 is biased to a potential VBE1 generated between the base and emitter of the transistor Q1. Here, the OP amp 600 absorbs a residual current obtained by subtracting an addition of the currents I1 and I3 from the current source I. The voltages V1 and V3 are thus equal to each other, so that the potential V1 is equal to VBE1 (col. 1 lines 11-40).

4. Claims 1 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Wilhelm (EP 1132795 – supplied by applicant).

Wilhelm discloses a bandgap reference voltage circuit (figure 2, paragraph 3) including a first amplifier (OP) having a first (+) and second (-) input and providing a voltage reference (Vb) at the output thereof, the amplifier being coupled at its first input to a first transistor and at the second input to a second transistor (n Emitter), the second transistor having an emitter area larger than that of the first transistor; the second transistor is coupled at its emitter to a load resistor, the load resistor providing, in use, a measure of the difference in base emitter voltages between the first and second transistors for use in the formation of the bandgap reference voltage; the bases of each transistor are commonly coupled such that they are at the same potential; one of the first and second transistors is provided in a diode connected configuration; and the base collector voltage of the other of the first and second transistors is maintained at zero by the amplifier

which is coupled in a feedback loop to the collector of each of the transistors, thereby reducing the Early effect.

Allowable Subject Matter

5. Claim 19 is allowed.

6. Claims 2-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: the reasons for indicating allowable subject matter remain the same as stated in the prior office action dated 11/17/04.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 6,677,808 Sean et al disclose a CMOS adjustable bandgap reference; US 6,411,158 Essig disclose a bandgap reference circuit.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary L. Laxton whose telephone number is (571) 272-2079. The examiner can normally be reached on Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2084. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

5/18/05

Gary L. Laxton
Primary Examiner
Art Unit 2838